## I claim:

1. A data-processing device for processing in parallel a plurality of independent processes, comprising:

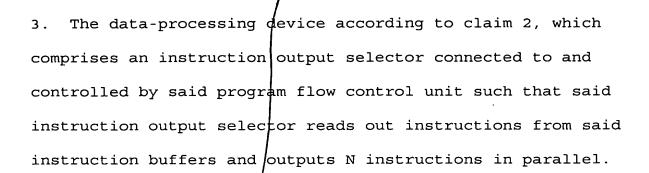
a program memory having stored therein at least one compiled program with a multiplicity N of independent processes, the compiled program including information on parallelism and a multiplicity of bundles with a plurality of instructions of a process;

a branching control unit connected to and addressing said program memory;

a register for storing flags and data which are switched in dependence on a process being executed; and

a program flow control unit connected to said branching control unit, said program flow control unit controlling a fetching of bundles from said program memory and said branching control unit and an output of instructions in dependence on information contained in the instructions and included in a compiling time of the program.

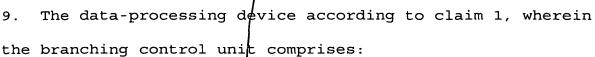
2. The data-processing device according to claim 1, which comprises a number N instruction buffers connected in parallel downstream of said program memory for storing instructions read out from said program memory.



- 4. The data-processing device according to claim 1, which comprises N instruction decoders for decoding the instructions being output.
- 5. The data-processing device according to claim 1, which comprises at least two instruction-execution units for outputting the N decoded instructions.
- 6. The data-processing device according to claim 5, which comprises a data memory and at least two buses connecting said .

  N instruction-execution units to said data memory.
- 7. The data-processing device according to claim 1, wherein said program flow control unit is configured to execute the instructions of one or more bundles in parallel.
- 8. The data-processing device according to claim 1, wherein said branching control unit is configured to output an address pointer for addressing a bundle.





a first multiplexer and a second multiplexer;

an adder; and

N program counters; and

wherein said program flow control unit feeds a number of instructions in a bundle to said adder and said adder adds an address pointer and the number of instructions;

wherein said program flow control unit feeds addresses for program jumps or function calls and a process number to said first multiplexer;

said first multiple er writing either the output signal of said adder or the addresses for program jumps or function calls into said program counter assigned to the active process; and

a content of said program counter assigned to the currently active process is output as a new address pointer via said second multiplexer which is controlled using the process number supplied.





- 10. The data-processing device according to claim 1, wherein said program flow control unit is configured to receive via a subbus of an output bus of said program memory at least one of the following:
- at least one bit for indicating the parallel execution of instructions;
- at least one bit for indicating the length of the following instruction bundle;
- the indication of or more NOPs in the instruction bundles;
- a priority of the processes of the instructions.
- 11. The data-processing device according to claim 1, wherein a process is called by assigning a process number, a priority and a memory address of a starting point of the process in the program memory.
- 12. The data-processing device according to claim 1, wherein said data-processing device is a network processor for processing layer 1 to 7 of protocol stacks in applications including LAN, ATM switches, IP routers, and frame relays based on a system selected from the group consisting of DSL, Ethernet, and cable modems.